



UP2000+  
Technical Reference Manual

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# Revision History

Date	Rev	Description
6/22/00	51-0039-1A	<b>UP2000+ Technical Reference Manual first product release. This manual describes the Alpha Processor, Inc. part number UP2000-B1.</b>
7/24/00	51-0039-1B	Add DDR Slot B support.

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# Preface

## Overview

This manual describes the Alpha Processor, Inc. UP2000+ product, including the UP2000+ Motherboard used with the Alpha Slot B Module, for computing systems based on Samsung's Alpha 21264 microprocessor and the Compaq 21272 core logic chipset.

## Audience

This manual is intended for system designers and others who use the UP2000+ to design or evaluate computer systems based on the Alpha Slot B Module with the 21264 microprocessor and the 21272 core logic chipset.

## Scope

This manual describes the functional operation, firmware platform and memory interfaces of the UP2000+. This manual does not include specific details on industry standards (for example, on PCI or ISA bus specifications). Additional information is available in the appropriate vendor and IEEE specifications. See Appendix B for information on how to order related documentation and obtain additional technical support.

## Manual Organization

The *UP2000+ Technical Reference Manual* is organized as follows:

- A functional description of the UP2000+ is provided in Chapter 1, "Functional Description." This includes the 21272 core logic chipset and a brief description of its implementation with the 21264 microprocessors.
- Chapter 2, "Firmware Platform," includes a description of the firmware components supported by the UP2000+ and the order in which these components load.
- Chapter 3, "System Memory and Address Mapping," provides a description of the memory subsystem and address mapping for the UP2000+.
- Pinouts for the Alpha Slot B Connectors are provided in Appendix A, "Alpha Slot B Connector Pinouts."

- Appendix B, “Support, Products and Documentation,” describes how to obtain technical information and support for the UP2000+, and where to order parts and accessories for the UP2000+. It includes information on how to obtain Alpha Processor, Inc. products and supporting literature.

## Conventions and Definitions

This section defines product-specific terminology, abbreviations, and other conventions used throughout this manual.

### Typographic Conventions

This manual uses the following type conventions:

- Variable information and document titles appear in *italic* type.
- Text that you type is shown in **bold Courier font**.
- Type that appears on a screen, such as an example of computer output, is shown in `Courier font`.
- Two key names joined with a forward slash are simultaneous keystrokes. Press down the first key while you type the second key, as in press `Ctrl/S`.

### Signals and Bits

- **Signal Ranges**—In a range of signals, the highest and lowest signal numbers are contained in brackets and separated by a colon (for example, `D[63:0]`).
- **Reserved Bits and Signals**—Signals or bus bits marked *reserved* must be driven inactive or left unconnected, as indicated in the signal descriptions. These bits and signals are reserved by Alpha Processor, Inc. for future implementations. When software reads registers with reserved bits, the reserved bits must be masked. When software writes to these registers, it must first read the register and change only the non-reserved bits before writing back to the register.

### Data

The following list defines data terminology:

- Units
  - A *word* is two bytes (16 bits)
  - A *doubleword* is four bytes (32 bits)
  - A *quadword* is eight bytes (64 bits)
- Addressing—Memory is addressed as a series of bytes on eight-byte (64-bit) boundaries in which each byte can be separately enabled.
- Abbreviations—The following notation is used for bits and bytes:
  - Kilo—K, as in 4-Kbyte page ( $2^{10}$ )
  - Mega—M, as in 4 Mbits/sec ( $2^{20}$ )
  - Giga—G, as in 4 Gbytes of memory space ( $2^{30}$ )

## Acronyms

The following is a list of the acronyms used in this document and their definitions.

Abbreviation	Meaning
BIST	Built-In Self Test
<b>CE</b>	<b>European Conforming</b>
CLI	Command Line Interface
<b>CSR</b>	<b>Control/Status Register</b>
CPU	Central Processing Unit
<b>CUL</b>	<b>Canadian Underwriters Laboratory</b>
DBM	Debug Monitor
<b>DIMM</b>	<b>Dual Inline Memory Module</b>
DMA	Direct Memory Access
<b>DRAM</b>	<b>Direct Random Access Memory</b>
DQM	Data Input/Output Mask
<b>EIDE</b>	<b>Enhanced Integrated Device Electronics</b>
EMI	Electromagnetic Interference
<b>EPLD</b>	<b>Electrically Programmable Logic Device</b>
ESBGA	Enhanced Super Ball Grid Array
<b>FCC</b>	<b>Federal Communications Commission</b>
FDC	Floppy Disk Controller
<b>FDD</b>	<b>Floppy Disk Drive</b>
FID	Frequency Identification
<b>FIFO</b>	<b>First In, First Out</b>

<b>Abbreviation</b>	<b>Meaning</b>
FPGA	Field Programmable Gate Array
<b>HDD</b>	<b>Hard Disk Drive</b>
I <sup>2</sup> C	Inter-integrated Circuit
<b>IDE</b>	<b>Integrated Device Electronics</b>
I/O	Input/Output
<b>ISA</b>	<b>Industry Standard Architecture</b>
ISP	In-system Programmability
<b>LED</b>	<b>Light Emitting Diode</b>
LVD	Low Voltage Differential
<b>LVTTTL</b>	<b>Low Voltage Transistor-Transistor Logic</b>
NDA	Non-disclosure Agreement
<b>OEM</b>	<b>Original Equipment Manufacturer</b>
OS	Operating System
<b>PAL</b>	<b>Privileged Architecture Library</b>
PCB	Printed Circuit Board
<b>PCI</b>	<b>Peripheral Component Interconnect</b>
PIO	Programmed Input/Output
<b>PLL</b>	<b>Phase Locked Loop</b>
ROM	Read-only Memory
<b>RTC</b>	<b>Real-time Clock</b>
SCSI	Small Computer System Interface
<b>SDRAM</b>	<b>Synchronous Direct Random Access Memory</b>
SE	Single-ended
<b>SPD</b>	<b>Serial Presence Detect</b>
SRAM	Serial Read-only Memory
<b>SRAM</b>	<b>Static Random Access Memory</b>
SRM	System Reference Manual
<b>SSRAM</b>	<b>Synchronous SRAM</b>
TIG	TTL Integrated Glue Logic
<b>UL</b>	<b>Underwriters Laboratory</b>
USB	Universal Serial Bus
<b>VRM</b>	<b>Voltage Regulator Module</b>

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# Chapter 1 Functional Description

This chapter describes the functional operation of the UP2000+. It introduces the 21272 core logic chipset and briefly describes its implementation with the 21264 microprocessors.

Descriptions are also provided in this chapter of the subsystem structure of the UP2000+, and the logic and firmware used.

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## 1.1 System Components

The UP2000+ is implemented in industry-standard parts and uses one or two 21264 central processing units (CPUs). The functional components of the UP2000+ are shown in block diagram form in Figure 1-1. A detailed description of system components is provided in Chapter 1, “Functional Description”

**Note:** Refer to the list of Acronyms on page x of the Preface for a definition of terminology used in the block diagram.

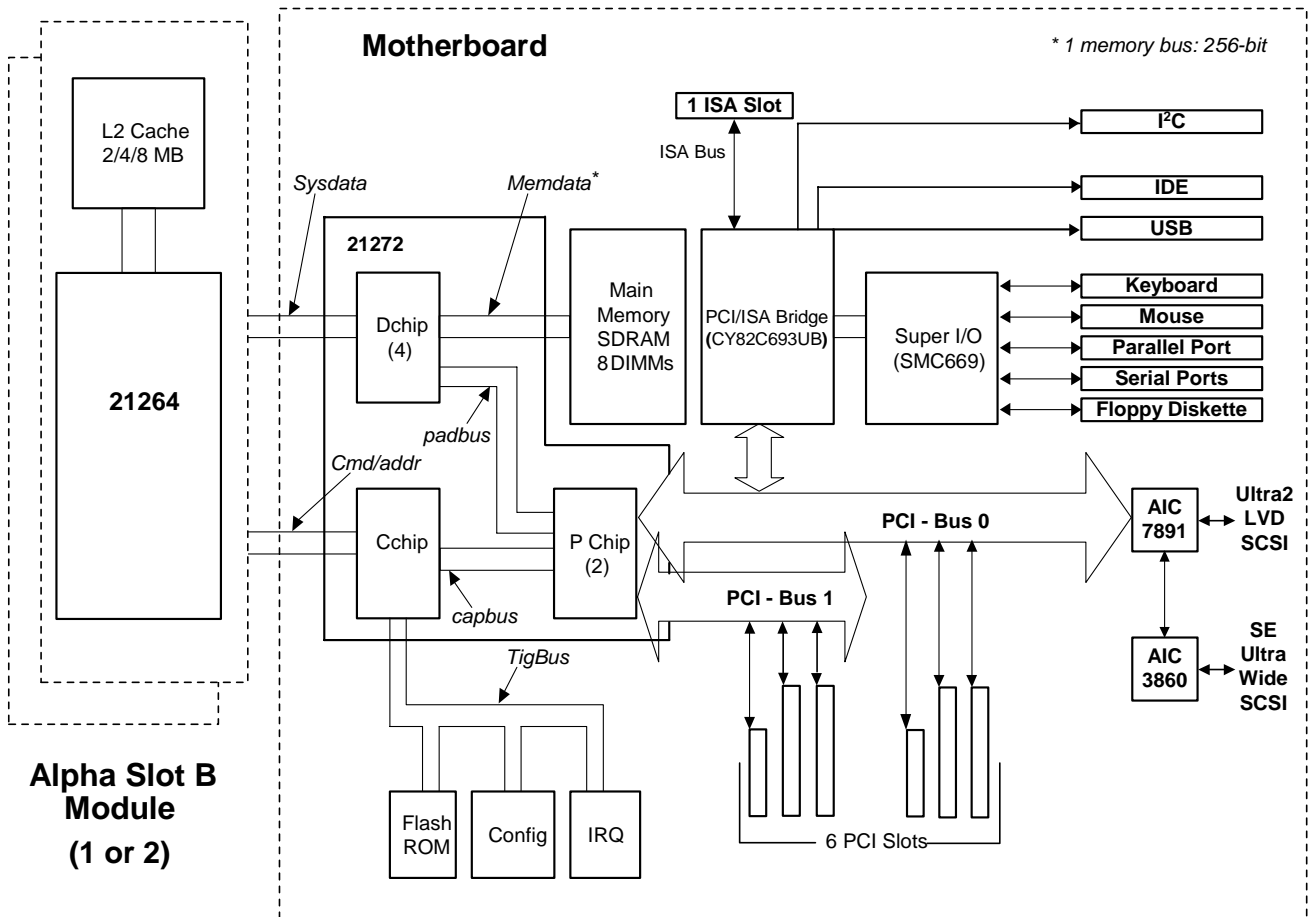


Figure 1-1 UP2000+ Functional Block Diagram

## 1.2 21272 Core Logic Chipset

The UP2000+ uses a Compaq 21272 (Tsunami) chipset to implement a uni-processor or dual-processor system based on the 21264 microprocessor, which is located on the Alpha Slot B Module. The chipset provides a 256-bit memory interface and includes the following three gate arrays:

- Cchip—controls address and commands, and is 432-pin Enhanced Super Ball Grid Array (ESBGA). The Cchip connects to the system interrupts by the TTL Integrated Glue Logic (TIG) block.
- Dchips—four 304-pin ESBGAs control the data path. Dchips provide the data path between the CPU, the memory and the Pchips.
- Pchips—two 304-pin ESBGAs control the PCI interface.

A 32-byte bus from the SDRAM arrays splits into two memory ports at the Dchips.

Refer to Compaq's documentation for a full explanation of the 21272 chipset.

## 1.2.1 Cchip Functional Overview

The Cchip provides the control interface between the Alpha Slot B Module, containing the 21264 microprocessor, and the UP2000+ Motherboard 21272 chipset. In addition, it provides control for the Dchips, Pchips, memory subsystem and access to the TIG block.

The CPU and the Cchip communicate with each other through the system port. The system port is made up of unidirectional address and command buses. The Cchip system interface logic decodes the system port address for CPU requests to determine what action to take. It also decodes Direct Memory Access (DMA) requests from the Pchips.

The Cchip supports cacheable memory accesses, programmed I/O, interrupts, TIG addresses, and accesses to 21272 control/status register (CSR) space.

## 1.2.2 Dchip Functional Overview

The Dchips provide the data path from the 21264 to main memory. Four Dchips are used for the interface on the UP2000+ Motherboard. The Dchips contain the CPU, Pchip, and memory interface data paths, which include DMA and Programmed Input/Output (PIO) queues.

The Dchips interface to the CPU using the system data bus (sysdata). The system data bus, between the Dchips and each CPU, passes 128 bits of data (64 bits, or 8 bytes, from each CPU).

There is also a 256-bit, bidirectional memory bus (memdata) between the Dchips and the memory banks. The memory bus connects to banks 0 and 1 (see Figure 1-4).

Dchips interface with each Pchip through the 32-bit PAD bus (PADbus; PADbus0 connects to Pchip 0 and PADbus1 connects to Pchip 1). The PADbus is a 32-bit data bus that allows a Pchip and the Dchips to pass data back and forth.

### 1.2.3 Pchip Functional Overview

The Pchip is a fully-compliant PCI host bridge between the PCI and the CPU and its cache and memory. Pchip interface protocol is compliant with *PCI Local Bus Specification, Revision 2.1*.

The Pchip contains all control functions of the PCI bridge and some data path functions. It acts as a master on the PCI for CPU-initiated transactions, and is a target on memory space transactions initiated by PCI masters. Two Pchips are used on the UP2000+ Motherboard to provide two 64-bit PCI buses.

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## 1.3 Subsystems

The following paragraphs describe the designs of the UP2000+ functional subsystems.

### 1.3.1 Memory Subsystem

The UP2000+ Motherboard has eight DIMM sockets arranged in two banks: bank 0 and bank 1. Each bank has four sockets and provides a 256-bit wide data path. DIMMs in the same bank must be the same type, size, and speed; DIMMs in different banks may differ in type, size, and speed. At least one memory bank must be filled for the UP2000+ Motherboard to work.

The UP2000+ supports memory DIMMs such as the sample list described in Table 1-1. This is not a comprehensive list of DIMMs supported. For current information on memory DIMM compatibility, refer to the Alpha Processor, Inc. website:

<http://www.alpha-processor.com/>

**Table 1-1 SDRAM DIMMs Supported**

<b>Vendor</b>	<b>Size</b>	<b>Vendor Part Number</b>
Samsung	<b>64 MB</b>	<b>KMM350S823BT1</b>
	64 MB	KMM377S823BT1
	<b>128 MB</b>	<b>KMM377S1620BT1</b>
	256 MB	KMM377S3320T1
	<b>256 MB</b>	<b>KMM377S3323T</b>
	256 MB Stack	KMM377S3227BT1
<b>Viking</b>	<b>128 MB</b>	<b>PE16721R4SN3-2226</b>

### 1.3.2 CPU (Alpha Slot B Module) Interface

The UP2000+ is designed to interface to one or two Alpha Slot B Modules. Two 330-pin connectors accept two Alpha Slot B Module connections for dual-21264 configuration. The board also works with a single Alpha Slot B Module connected, with the secondary Alpha Slot B Module connector left open.

The Alpha Slot B Connector provides signal pins (154 total), 5 Volt pins (2A), 3.3 Volt pins (8A), 2V\_TERM (58A), static RAM (SRAM) power pins (2A), and ground pins (70 total) from the UP2000+ Motherboard. The VRM power source, connected on odd-numbered pins between 145–165, is auto-switched between 12V and 5V.

Alpha Slot B Module interface specifications are as follows:

- Molex part number: 74191-0002
- Designed for signal transmissions with rise and fall times of 0.5 nsec or greater
- Current rating: Signal contact = 1A, Ground contact = 1.5A

### 1.3.3 Clock Subsystem

The CPU and system clock frequency is decided by the UP2000+ Motherboard's external PLL logic and the CPU internal PLL logic. The external PLL logic provides the reference clock input to the CPU and the 21272 chipset.

All external and internal PLL input parameters are set by TIG Field Programmable Gate Array (FPGA) logic configured by the UP2000+

Motherboard reset logic. This TIG FPGA has an internal PLL look-up table used to set the value of M[6:0] and N[1:0], which are input parameters of external PLL devices, and the value of Y-divider, which is an input parameter of CPU internal PLL logic.

These input values of the external PLL device are set through the TIG FPGA device using Inter-integrated Circuit (I<sup>2</sup>C) protocol.

Table 1-2 describes how the input parameters of external PLL are set.

**Table 1-2 PLL Input Frequency**

External PLL Output Freq.	M[6:0] Value	N[1:0] Value
<b>83 MHz</b>	<b>28h</b>	<b>10b</b>
133 MHz	20h	01b
<b>150 MHz</b>	<b>24h</b>	<b>01b</b>
166 MHz	28h	01b

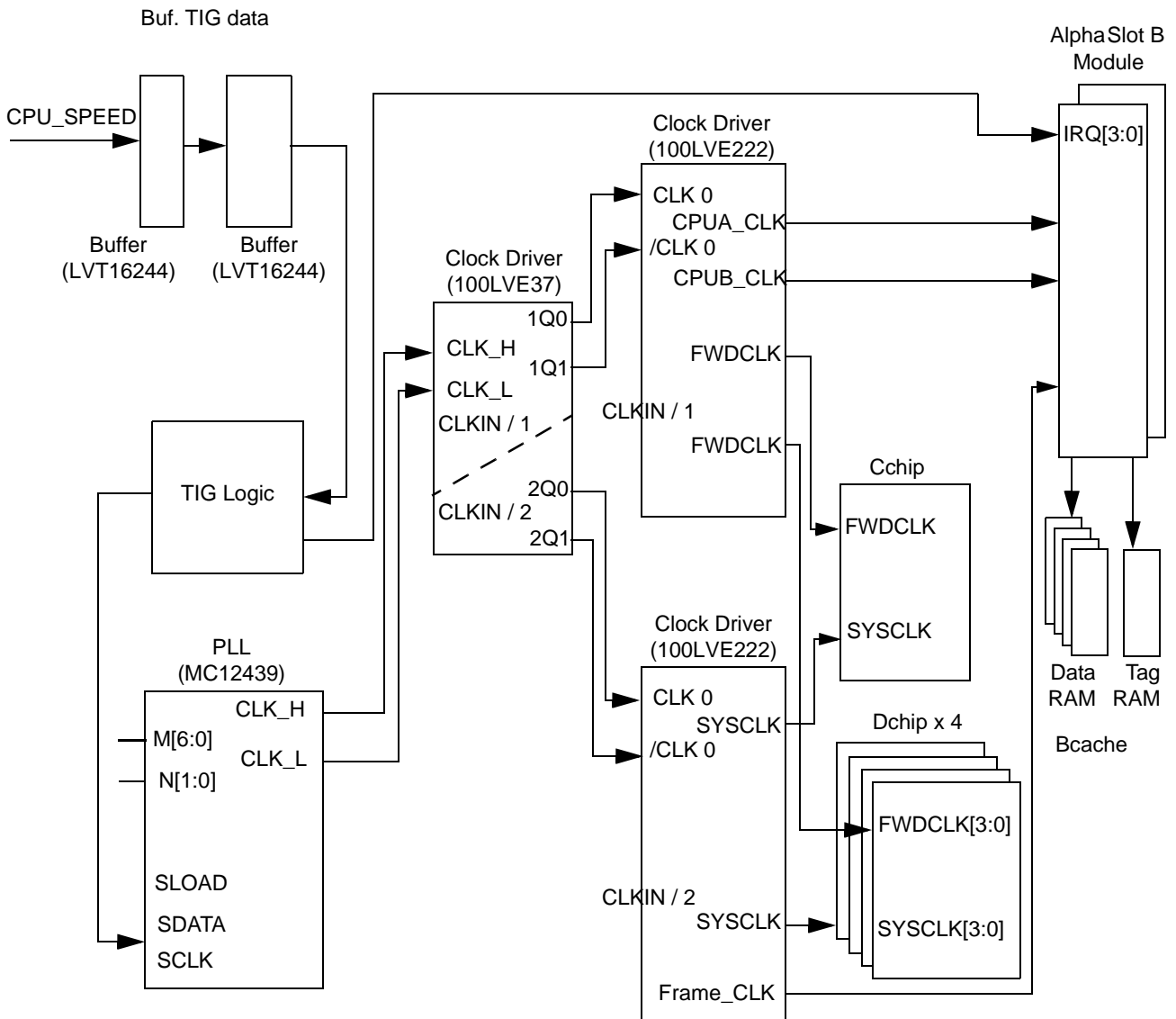
The output frequency of this external PLL device is used as the CPU reference clock and system clock of the UP2000+. The CPU reference clock produces the internal processor clock [GCLK] through internal PLL logic and the Y-divider value, which is multiplied as shown in Table 1-3.

**Table 1-3 Reference, CPU and PCI Clocks**

Alpha Slot B Module	Used Speed	Y Divider	CLKin	PCI Clock
<b>667 MHz</b>	<b>666 MHz</b>	<b>4</b>	<b>166 MHz</b>	<b>33 MHz</b>
750 MHz	750 MHz	5	150 MHz	30 MHz
<b>833 MHz DDR</b>	<b>833 MHz</b>	<b>5</b>	<b>166 MHz</b>	<b>33 MHz</b>

*Note: The Y-divider value is set through IRQ[3:0] input signals and configured by the TIG FPGA internal PLL look-up table.*

The CPU and system clock design is shown in block diagram form in Figure 1-1.



**Figure 1-1 CPU and System Clock Block Diagram**

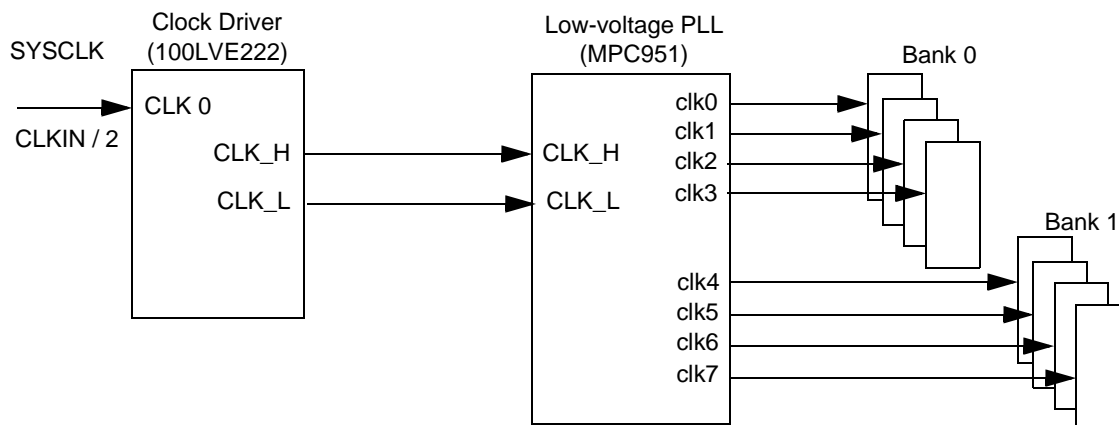
The LVE37 clock driver receives PLL clock signals, and performs an  $\times 1$  or  $\times \frac{1}{2}$  operation and sends the output to the LVE222 clock driver (1:15 differential  $\times 1$  or  $\times \frac{1}{2}$ ). The  $\times 1$  clock is sent to LVE222 for the CPU clock and for the forward clock drive for each chipset, and  $\times \frac{1}{2}$  clock is sent to the other LVE222 for system clock for each chipset.

**Memory Interface Clock**

The low voltage PLL clock driver (MPC951), which received system clock through the clock drive, goes through each DIMM as 1:1 clock output. One clock is used as a feedback clock to reduce the skew.

There are a total of nine clock outputs. Since the 168-pin DIMM used in the UP2000+ is registered (including PLL), only one clock source is needed to do the loading.

Figure 1-2 shows a block diagram of the UP2000+ memory interface clock design.



**Figure 1-2 Memory Interface Clock Block Diagram**

**PCI Clock**

The set value of the internal register PCLKX determines which divide ratio the Pchips use for dividing the forward clock signal. Refer to Table 1-4 for a list of the divide ratio values.

**Table 1-4 PCI Clock Frequency Multiplier**

PCLKX	Forward Clk Divide Ratio
0	6
1	4
2	5

Pchip register PCTL contains PCLKX[41:40], which can be used to configure the PCI clock frequency multiplier.

The PCLKX value is set in the SROM code. The value is used when the SROM code starts initializing the Pchip when the code goes into the Icache (instruction cache) of the CPU.

Refer to Figure 1-3 for a block diagram of the PCI clock design.

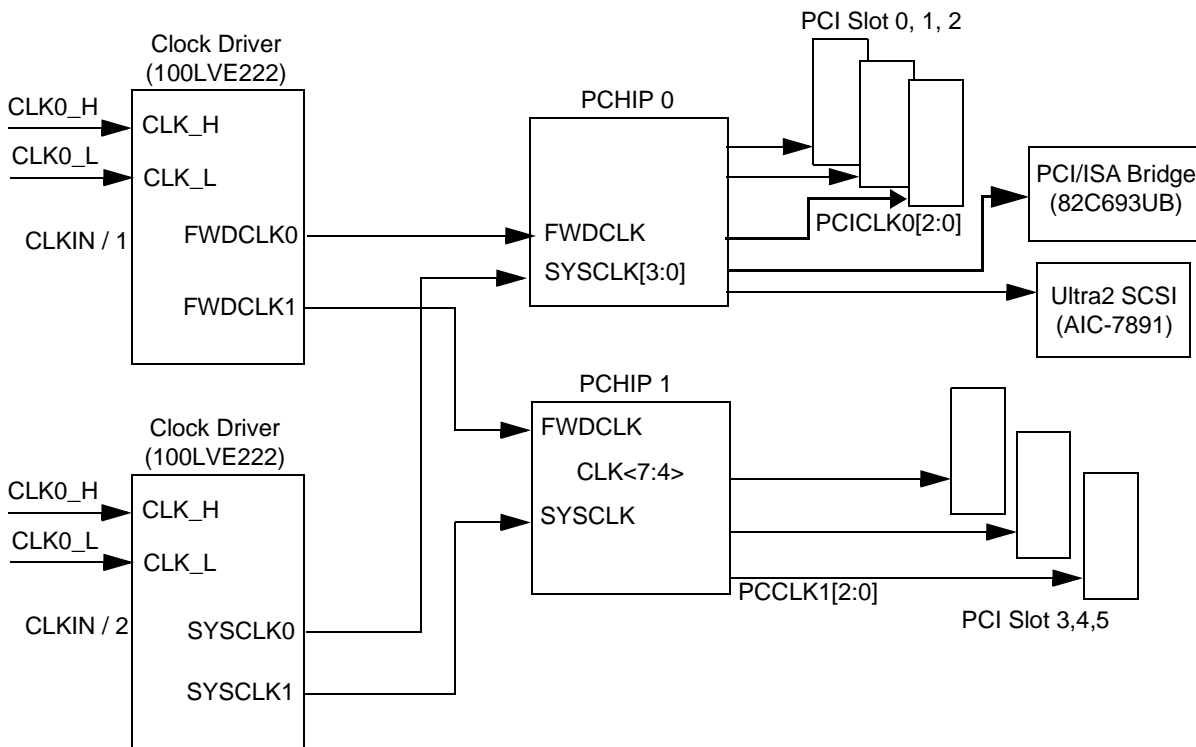


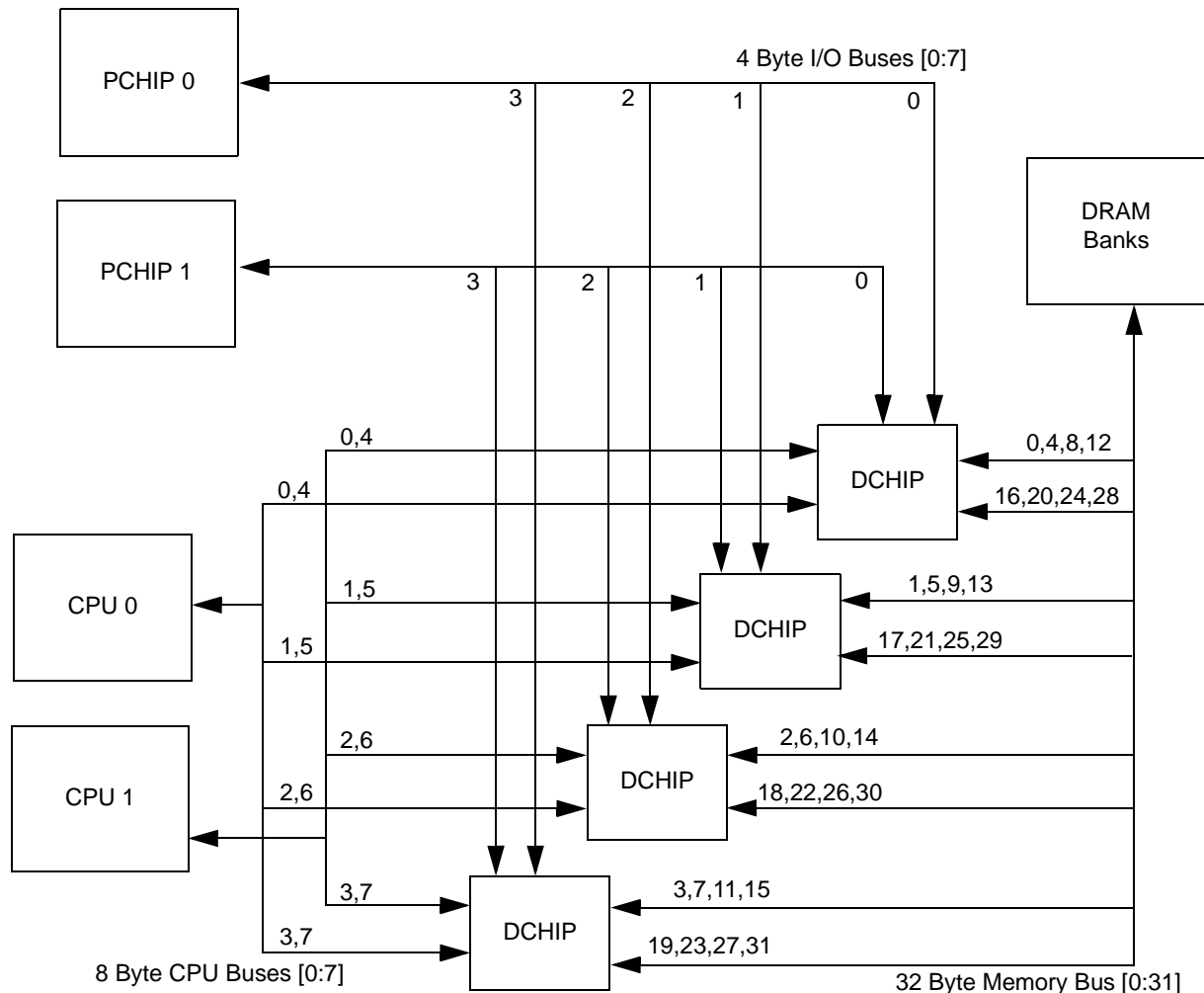
Figure 1-3 PCI Clock Generation Block Diagram

### 1.3.4 System Bus

The clock speed of the bus between the CPU and the chipsets is set up as 83 MHz.

The maximum bandwidth is designed as 2.67 GBytes/second. The bus between CPU and Dchips is designed as a 64-data bit bus, and the bus between Dchips and memory is designed as a 1-bus, 2-bank, and 32-byte bus.

Figure 1-4 shows a block diagram of the system bus design.



**Figure 1-4 System Bus Block Diagram**

The UP2000+ has two CPU buses with an 8-byte data width, and one memory bus with a 32-byte data width. This is accomplished by using one Cchip, four Dchips and two Pchips. Each of the synchronous dynamic RAM (SDRAM) banks is split into two memory ports of the Dchips. A cache block is read or written to the memory using two transfers on this bus. Each Dchip supplies two bytes to each installed CPU.

The instantaneous peak data transfer rates between the Dchips and the DRAM bank is 32 Bytes at 83 MHz, which is equal to 2.67 GB/sec. The instantaneous peak transfer rates between the CPUs and Dchips is 8 Bytes at 333 MHz (that is, a 167 MHz, double data rate), which is also equal to 2.67 GB/sec. The interface between Pchips and Dchips is 4 bytes at 83.3 MHz, which results in an instantaneous peak data transfer rate of 333 MB/sec.

### 1.3.5 PCI Interface

The UP2000+ supports six PCI slots (four 64-bit and two 32-bit) and one shared PCI/ISA slot. The PCI interface has a 33 MHz system clock. The UP2000+ also provides a PCI-to-ISA bridge (CY82C693UB). The on-board AIC-7891 has up to 80 MB/sec data transfer rates and a 64-bit PCI interface.

The primary Pchip is connected to the CY82C693UB PCI/ISA bridge, the Ultra2 SCSI Controller (AIC-7891), two 64-bit PCI slots, and one 32-bit PCI slot.

The secondary Pchip is connected to two 64-bit PCI slots and one 32-bit PCI slots.

#### Primary PCI Bus

The primary PCI bus (bus 0) has the following interconnections, as described in Table 1-5 and Table 1-6:

- Two 64-bit, 5V PCI slots
- One 32-bit, 5V PCI slot
- One CY82C693UB PCI/ISA bridge interface
- One AIC-7891 Ultra2 SCSI controller interface

**Table 1-5 PCI 0 Configuration ID**

IDSEL Value	Device
AD16	CY82C693UB
AD17	AIC-7891
AD18	PCI Slot 0 (64-bit)
AD19	PCI Slot 1 (64-bit)
AD20	PCI Slot 2 (32-bit)

**Table 1-6 Primary PCI Arbitration**

Arbitration Signals	Device Connected
P_REQ0#/P_GNT0#	CY82C693UB
P_REQ1#/P_GNT1#	AIC-7891
P_REQ2#/P_GNT2#	PCI Slot 0
P_REQ3#/P_GNT3#	PCI Slot 1
P_REQ4#/P_GNT4#	PCI Slot 2

Secondary PCI Bus      The secondary PCI bus (bus 1) has two 64-bit and one 32-bit 5V PCI slots, as described in Table 1-7 and Table 1-8.

**Table 1-7    PCI 1 Configuration ID**

IDSEL Value	Device
AD18	PCI Slot 3 (64-bit)
AD19	PCI Slot 4 (64-bit)
AD20	PCI Slot 5 (32-bit)

**Table 1-8    Secondary PCI Arbitration**

Arbitration Signals	Device Connected
P_REQ0#/P_GNT0#	PCI Slot 3
P_REQ1#/P_GNT1#	PCI Slot 4
P_REQ2#/P_GNT2#	PCI Slot 5
P_REQ4#/P_GNT4#	Not Used

### 1.3.6    On-Board I/O

The on-board I/O provided on the UP2000+ Motherboard are defined in Table 1-9.

**Table 1-9    On-board I/Os**

I/O Component	Specification
<b>FDC37C669</b>	• 2.88 MB floppy disk controller
	• Two Serial ports, NS16C550 compatible
	• One Parallel port

**Table 1-9 On-board I/Os (Continued)**

I/O Component	Specification
CY82C693UB	<ul style="list-style-type: none"> <li>• PCI-to-ISA bridge, <i>PCI Local Bus Specification Revision 2.1</i> compliant</li> </ul>
	<ul style="list-style-type: none"> <li>• <b>DMA controllers with type A, B, and F support</b></li> </ul>
	<ul style="list-style-type: none"> <li>• Interrupt controllers</li> </ul>
	<ul style="list-style-type: none"> <li>• <b>Timer/counters</b></li> </ul>
	<ul style="list-style-type: none"> <li>• Real-time clock with 256 bytes of battery-backed SRAM</li> </ul>
	<ul style="list-style-type: none"> <li>• <b>Dual-channel, EIDE controller with PCI bus mastering, CD-ROM support, PIO modes 0 through 4 operation, and single-word and multi-word DMA modes 0 through 2</b></li> </ul>
	<ul style="list-style-type: none"> <li>• Keyboard and mouse controller</li> </ul>
	<ul style="list-style-type: none"> <li>• <b>PCI-ISA/ISA-PCI/IDE-PCI/PCI-IDE post writing</b></li> </ul>
	<ul style="list-style-type: none"> <li>• USB controller</li> </ul>
	<ul style="list-style-type: none"> <li>• <b>Two USB ports</b></li> </ul>
AIC-7891 (SCSI Controller)	<ul style="list-style-type: none"> <li>• Supports Ultra2 LVD devices with 80 Mbyte/sec data transfer rate in 16-bit mode or 40 MByte/sec in 8-bit mode.</li> </ul>
	<ul style="list-style-type: none"> <li>• <b>Supports Ultra-wide Single-ended SCSI devices with an additional driver IC, AIC-3860</b></li> </ul>
	<ul style="list-style-type: none"> <li>• 512-byte data First In, First Out (FIFO) buffer for efficient PCI bus utilization</li> </ul>
	<ul style="list-style-type: none"> <li>• <b>PCI-tagged command queuing allows changes in the order of SCSI command execution</b></li> </ul>
	<ul style="list-style-type: none"> <li>• Connection for up to 15 SCSI devices on 12 meter cable</li> </ul>

Refer to Figure 1-5 for a block diagram of the SCSI controller design.

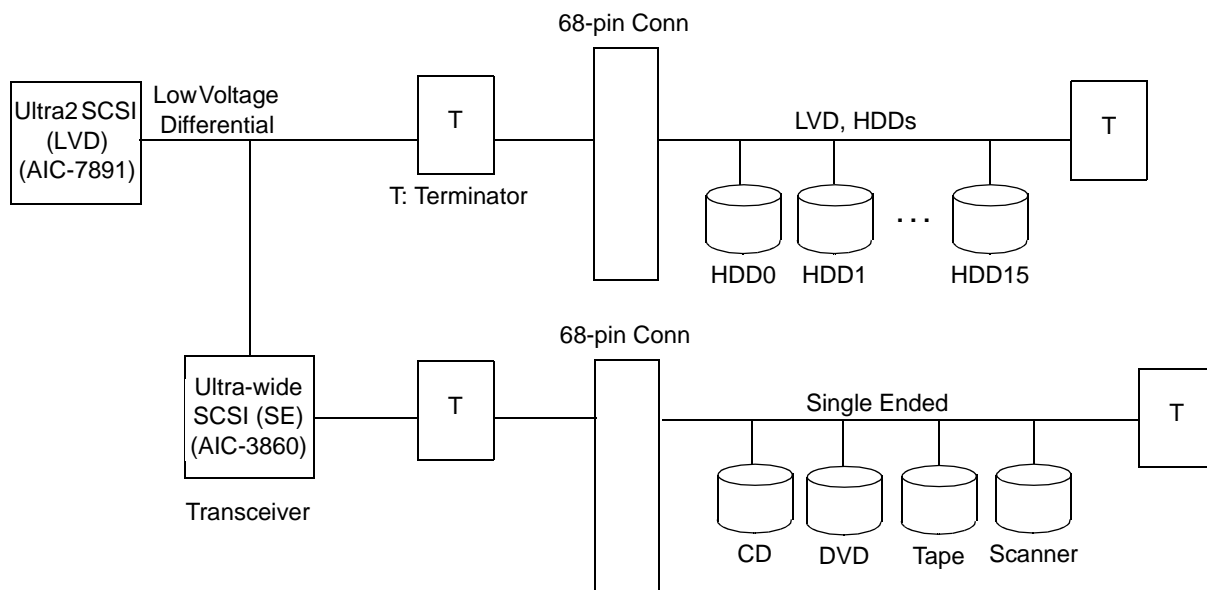


Figure 1-5 SCSI Controller Block Diagram

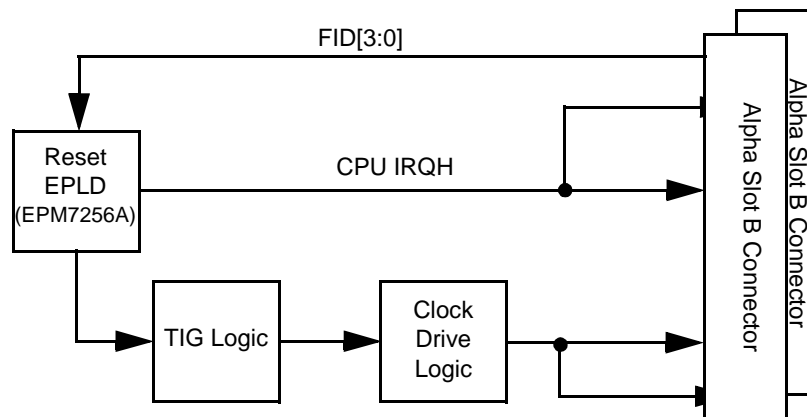
## 1.4 Logic

### 1.4.1 CPU Speed Logic

The CPU speed is set by the Y-divider value sent on the initial IRQH signal input through the interrupt bus. CPU speed is determined by the FID value from the Alpha Slot B Module.

**Note:** The UP2000+ only supports the use of the same speed CPUs on both processors.

A diagram of the CPU speed logic is shown in Figure 1-6.



**Figure 1-6 CPU Speed Logic**

## 1.4.2 Interrupt Logic

The TIG FPGA decoder divides a total of 64 interrupt sources by eight, then transfers them through the TIGbus.

The UP2000+ receives the thermal sensor interrupt signal I2C\_INTR\_L from each Alpha Slot B Connector, and uses a flip-flop design to support the interrupt even if only one interrupt is received.

The UP2000+ was designed to support only one on-board SCSI controller interrupt. It uses the AIC-7891, which supports one LVD port, and the AIC3860, which supports one single-ended port.

A block diagram of the interrupt logic design is shown in Figure 1-7. Table 1-10 provides a map of the UP2000+ logical interrupts.

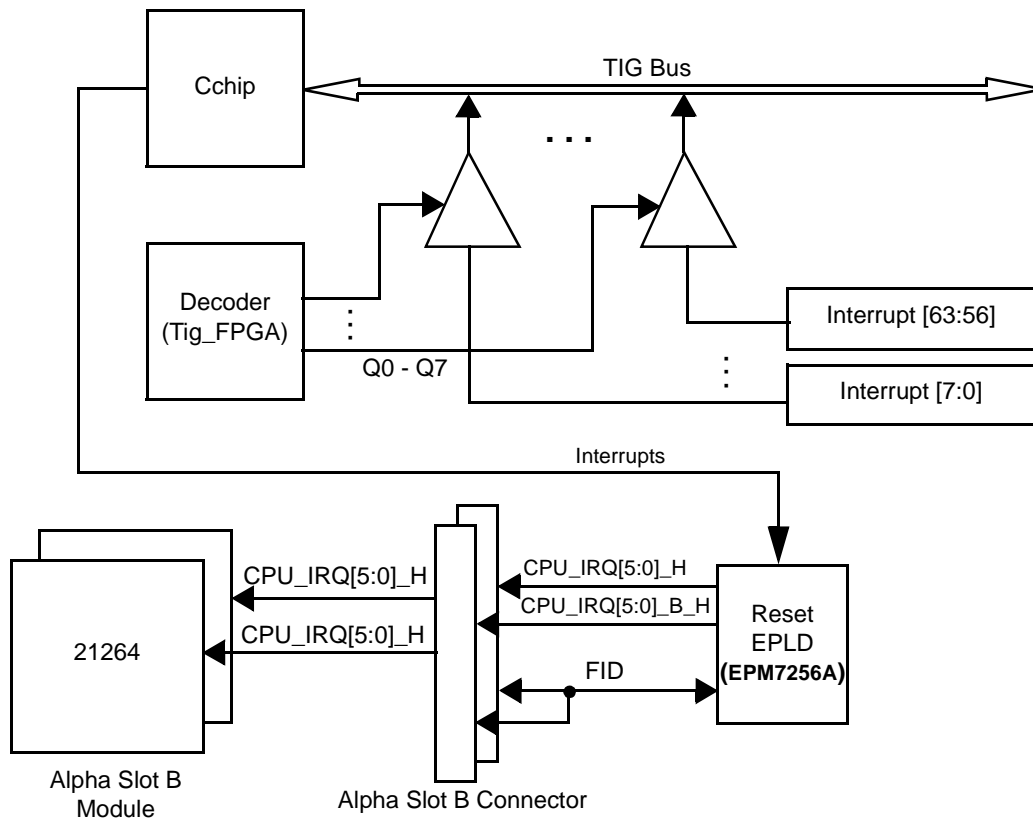


Figure 1-7 Interrupt Logic Block Diagram

Table 1-10 Logical Interrupt Map

INT_EN	Interrupt Level	Signal Name
INT_EN0	16	Reserved
	17	I2C_INT I2C Controller (PCF8584)
	18	Reserved
	19	PCI0_IRQ_ADPTA
	20	PCI0_INTD2
	21	PCI0_INTC2
	22	PCI0_INTB2
	23	PCI0_INTA2

**Table 1-10 Logical Interrupt Map (Continued)**

<b>INT_EN</b>	<b>Interrupt Level</b>	<b>Signal Name</b>
INT_EN1	24	PCI0_INTD1
	25	PCI0_INTC1
	26	PCI0_INTB1
	27	PCI0_INTA1
	28	PCI0_INTD0
	29	PCI0_INTC0
	30	PCI0_INTB0
	31	PCI0_INTA0
INT_EN2	32	PCF85741 (Secondary)
	33	PCF85740 (Primary)
	34	ADM92401 (Secondary)
	35	ADM92400 (Primary)
	36	PCI1_INTD2
	37	PCI1_INTC2
	38	PCI1_INTB2
INT_EN3	39	PCI1_INTA2
	40	PCI1_INTD0
	41	PCI1_INTC0
	42	PCI1_INTB0
	43	PCI1_INTA0
	44	PCI1_INTD1
	45	PCI1_INTC1
	46	PCI1_INTB1
INT_EN4	47	PCI1_INTA1
	48	Reserved
	49	Reserved
	50	THERM_WARN (Alpha Slot B Module Thermal Interrupts)
	51	Reserved
	52	Reserved
	53	CYP_NMI
	54	SMI_INT
	55	ISA_INT

**Table 1-10 Logical Interrupt Map (Continued)**

INT_EN	Interrupt Level	Signal Name
	<b>56</b>	<b>Reserved</b>
	57	Reserved
	<b>58</b>	<b>Reserved</b>
INT_EN5	59	Reserved
	<b>60</b>	<b>Reserved</b>
	61	PCI1_ERROR
	<b>62</b>	<b>PCI0_ERROR</b>
	63	Reserved

### 1.4.3 SRAM Code Access Logic

Reset EPLD supplies the SRAM code data to initialize the CPUs at reset. The FID value from the Alpha Slot B Module determines the appropriate flash select value. This flash select value determines which of the eight SRAM code images stored in flash ROM is sent to the CPU. The CPU holds the SRAM code output enable signal until the data load is complete.

Reset EPLD performs the following steps to load each CPU:

1. Dcok\_A\_H becomes active with Power\_on\_reset.
2. After Dcok\_A\_H is input, CPU0 holds about 8 GCLK cycles and the real EV6CLK\_x cycle occurs.
3. The Reset EPLD receives Mod\_reset, then sends Real\_reset\_A\_L to the CPU.
4. The CPU0 which receives Real\_reset\_A\_L finishes the PLL setting and enables Srom\_En\_A\_L.
5. The Reset EPLD which receives Srom\_En\_A\_L checks whether CPU1 is present.
  - If one CPU is used (CPU0 only):
    - a. Reset EPLD bypasses Srom\_En\_A\_L and sends the signal to the Cchip.
    - b. When the Cchip receives this signal, it enables ClkFwdRst\_H.
    - c. The CPU which received ClkFwdRst\_H performs Built-in Self Test (BIST), and loads SRAM\_Data into the CPU Icache.
    - d. After loading SRAM\_Data, the CPU deasserts Srom\_En\_L.
    - e. The Cchip checks this signal, and finishes it by deasserting ClkFwdRst\_H.
  - If two CPUs are used (CPU0 and CPU1):
    - a. After Srom\_En\_A\_L is input, SRAM\_Data finishes loading into

the Icache of CPU0, and Srom\_En\_A\_L is deasserted. This Srom\_En\_A\_L signal is latched so that the enabled signal goes into the Cchip.

- b. When Srom\_En\_A\_L is deasserted in the Reset EPLD internally, it enables Dcok\_B\_H and Real\_reset\_B\_L.
- c. When Srom\_En\_B\_L goes into Reset EPLD after being enabled, the Reset EPLD bypasses the signal and sends it to the Cchip.
- d. At this time, Reset EPLD deasserts the Real\_reset\_B\_L which is latched. This causes both CPUs to enter RUN mode (that is, the execution of SROM code data) at the same time by receiving ClkFwdRst\_H from the Cchip.

In other words, Reset EPLD receives Srom\_En\_L of the primary Alpha Slot B Module and maintains the signal low until the SROM code data gets loaded into the Icache of the secondary Alpha Slot B Module. After SROM code data is finished loading by both Alpha Slot B Modules, Srom\_En\_L is deasserted in both Alpha Slot B Modules at the same time to initialize the CPUs.

Reset EPLD is an ALTERA EPM7256A, 144-Pin ISP type component. Input Clock uses the CY2081 output clock of 14.318 MHz.

Figure 1-8 provides a diagram of the SROM code access logic design used in the UP2000+.

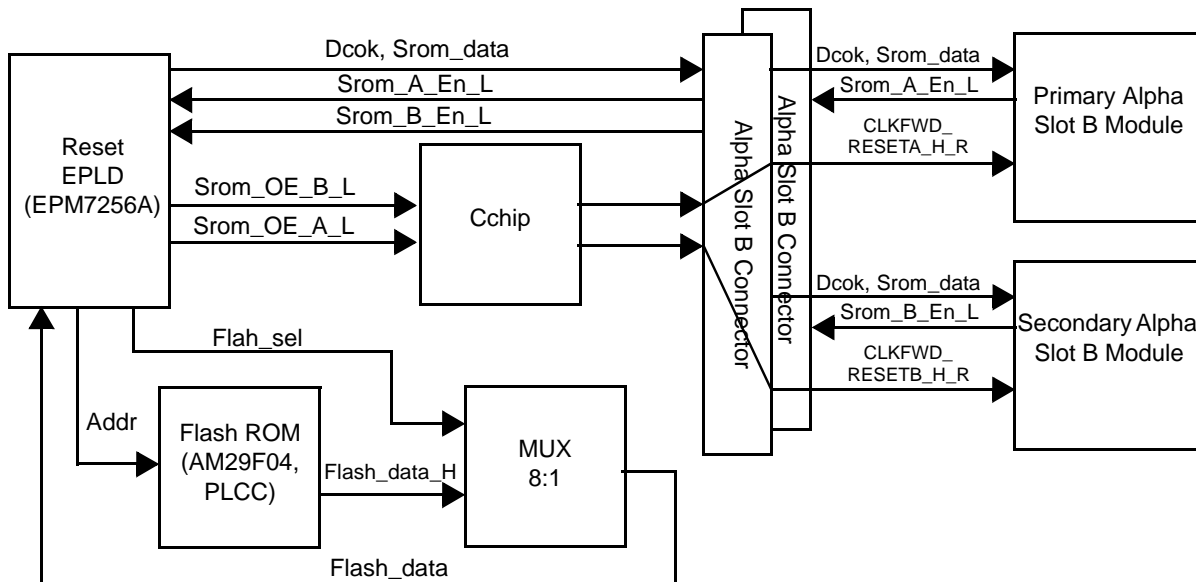


Figure 1-8 SROM Code Access Logic

### 1.4.4 On-board LED Logic

Six LEDs are used to indicate the status of the SROM\_CLK, DC\_OK, and 2V PWRGOOD signals on both the primary and secondary Alpha Slot B

Modules. One LED is used to indicate that the power supply is functioning correctly.

Figure 1-9 provides a diagram of the LED locations. All seven LEDs are located on the front edge of the UP2000+ Motherboard, to the left of the secondary Alpha Slot B Module. Table 1-11 describes the LED functions.

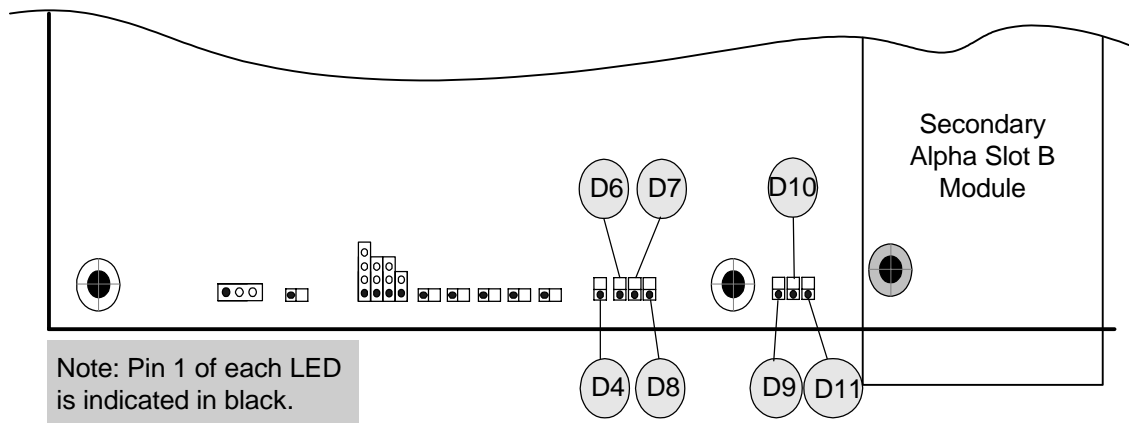


Figure 1-9 LED Locations

Table 1-11 LED Functions

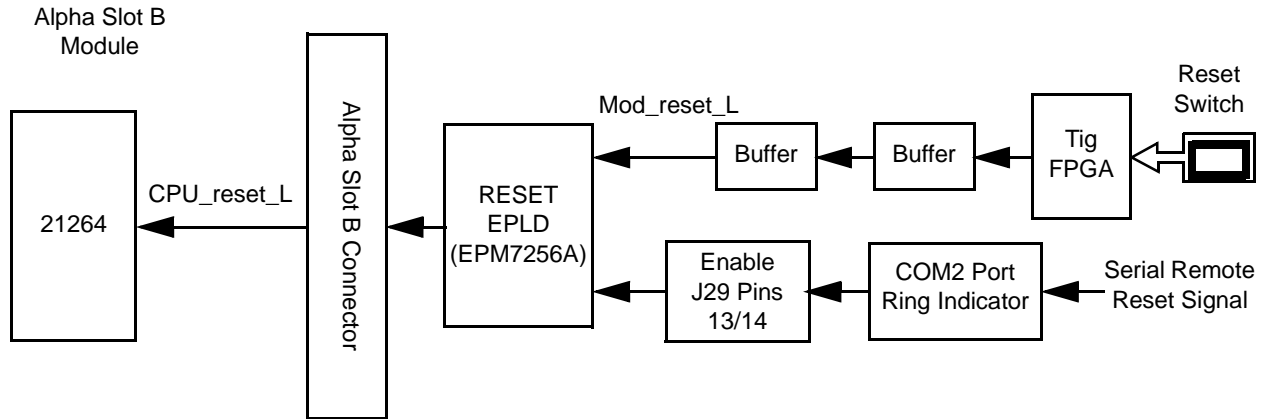
LED	Function
D4	PSU Power Good
D6	Secondary Alpha Slot B Module DC_OK
D7	Secondary Alpha Slot B Module SROM_CLK
D8	Secondary Alpha Slot B Module PWRGOOD
D9	Primary Alpha Slot B Module DC_OK
D10	Primary Alpha Slot B Module SROM_CLK
D11	Primary Alpha Slot B Module PWRGOOD

### 1.4.5 Alpha Slot B Connector Logic

Both Alpha Slot B Connectors use a 330-pin Molex connector, designed to support 12V and 5V. The primary Alpha Slot B Connector is hardwired with 12V and the secondary Alpha Slot B Connector is hardwired with 5V.

### 1.4.6 Reset Logic

The UP2000+ reset logic starts from the Power OK signal of the power supply. The processor reset starts from the Alpha Slot B Module reset FPGA logic. System reset and peripheral I/O reset signals are derived from the Cchip as shown in Figures 1-10 and 1-11.



**Figure 1-10 Alpha Slot B Module Reset Logic**

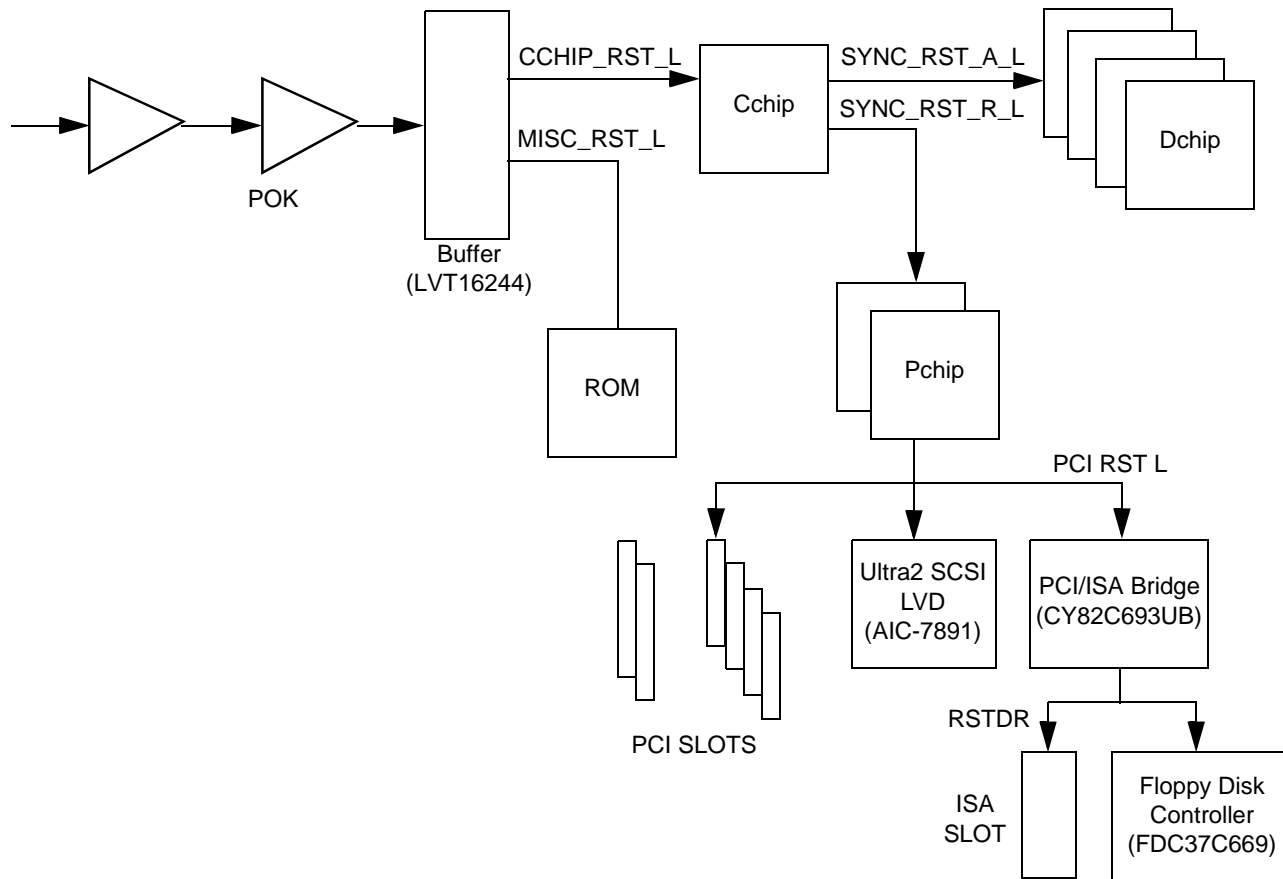


Figure 1-11 System Reset Logic

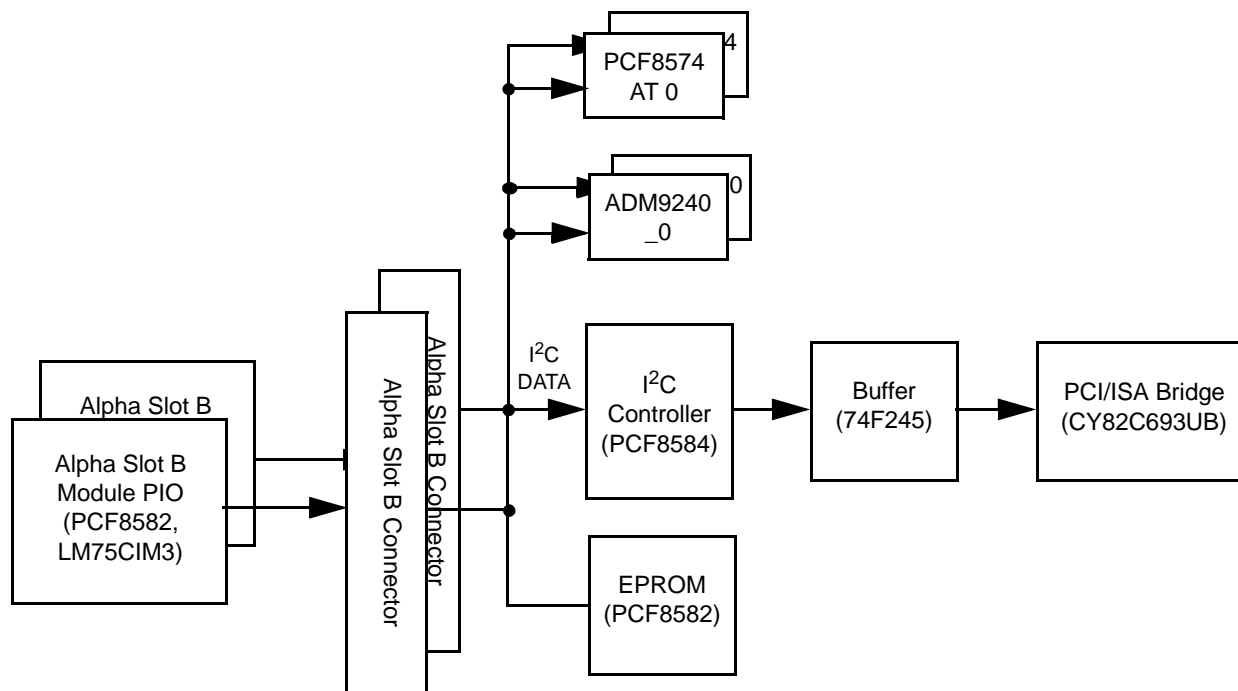
### 1.4.7 I<sup>2</sup>C Logic

#### System I<sup>2</sup>C Bus

The I<sup>2</sup>C controller (PCF8584) changes serial I<sup>2</sup>C data from the Alpha Slot B Modules to parallel signals, then sends them to the PCI/ISA bridge interface. This represents the system I<sup>2</sup>C logic bus. Table 1-12 shows the address mapping of the PCF8582C I<sup>2</sup>C EPROM and the LM75CIM3 thermal sensor. Figure 1-12 provides a diagram of the system I<sup>2</sup>C bus logic used in the UP2000+.

**Table 1-12 System I<sup>2</sup>C Address Map**

Component	Primary Alpha Slot B Module	Secondary Alpha Slot B Module	On-board
PIO PCF8582C	1010010	1010110	1010001
PIO LM75CIM3 thermal sensor	1001010	1001110	
<b>ADM9240 0 (Primary)</b>			<b>0101100</b>
ADM9240 1 (Secondary)			0101101
<b>PCF8574AT 0 (Primary)</b>			<b>0100000</b>
PCF8574AT 1 (Secondary)			0100001



**Figure 1-12 System I<sup>2</sup>C Bus Logic**

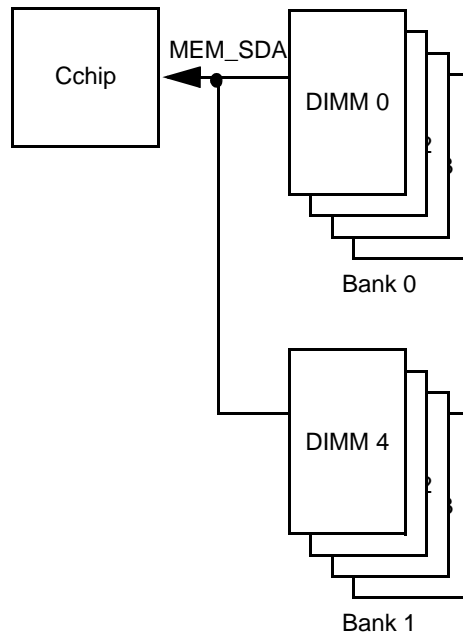
**Memory I<sup>2</sup>C Bus**

The UP2000+ also supports the memory DIMM I<sup>2</sup>C data from the I<sup>2</sup>C controller in the PCI/ISA bridge interface, which is represented as the memory I<sup>2</sup>C logic bus. Table 1-13 shows the address mapping of the

SDRAM SPD EEPROM. Figure 1-13 provides a diagram of the memory I<sup>2</sup>C bus logic used in the UP2000+.

**Table 1-13 Memory I<sup>2</sup>C Address Map**

Component	Memory Bank 0	Memory Bank 1
SDRAM SPD EEPROMs	1010000—DIMM 0	1010100—DIMM 4
	1010001—DIMM 1	1010101—DIMM 5
	1010010—DIMM 2	1010110—DIMM 6
	1010011—DIMM 3	1010111—DIMM 7



**Figure 1-13 Memory I<sup>2</sup>C Bus Logic**

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# Chapter 2 Firmware Platform

This chapter describes the UP2000+ target operating system (OS), and the SROM code, Alpha Diagnostics, and Alpha SRM console firmware. A description is included of the order in which firmware loads.

---

## 2.1 Supported Firmware

The UP2000+ supports the following firmware versions:

- SROM code—version 1.9.3 or higher
- Alpha Diagnostics—version 1.1 or higher
- Alpha SRM Console—version A5.5-82 or higher

### 2.1.1 OS

The UP2000+ supports Linux kernels 2.2.14 or higher.

**Note:** Refer to product support at the Alpha Processor, Inc. website for current information on specific distributors and OS versions supported by the UP2000+.

### 2.1.2 SROM Code

When the UP2000+ is turned on or reset, SROM code automatically loads into Icache in the CPU. This SROM code performs the following:

1. Initialize CPU.
2. Initialize CSR values—memory timing, Cchip, Dchip, and Pchip values.
3. Detect configuration jumpers, CPU configuration setting, and memory.
4. Initialize Bcache and set core logic chipset CSRs according to configuration.  
**Note:** In the 21272 chipset, there are 23 CSRs for the Cchip, 4 CSRs for the Dchips, and 48 CSRs for the Pchips.
5. Initialize system memory.
6. Detect CPU speed by polling of Periodic Interrupt Flag in the RTC.
7. Load the next level of firmware and pass control to that code. (See section 2.2, "Firmware Loading Order.")

Each Alpha Slot B Module requires a specific SROM code image, depending on the CPU speed. CPU speed is supplied by the FID value

determined by the Alpha Slot B Module.

**Note:** *If you use two Alpha Slot B Modules, both modules must use the same CPU speed. This means that both Alpha Slot B Modules also use the same SROM code.*

### 2.1.3 Alpha Diagnostics

The Alpha Diagnostics firmware is used internally by Alpha Processor, Inc. for diagnostic purposes.

Native mode diagnostics depends on various system components to be functioning correctly. When SROM code determines that the UP2000+ is capable of supporting the higher level environment, it fetches this image from the firmware and transfers control to it.

An Alpha Slot B Module using an 21264 processor implements a serial communications link directly connected to the processor. This link, called the Debug Port, can be used for reporting and interacting in the earliest stages of system initialization, after execution passes from PAL mode. It is accessed through J43 (primary) or J42 (secondary) on the UP2000+ Motherboard (see the *UP2000+ User Manual*, P/N 51-0042).

The Alpha Diagnostics firmware includes the following tests:

- Interrupt handling—Raise interrupts with a known response
- UP2000+ Motherboard components—chipset, Flash ROM integrity, on-board devices
- Memory—stress test
- ISA cards
- PCI bus—Initialization, stressing and interrupts
- SM timer support and EEPROMs
- FDD and IDE disks—DMA

If the Alpha Diagnostics detects a working keyboard and video console, it displays a graphical interface containing a menu of diagnostics. This is the console interface to the Alpha Diagnostics. If the Alpha Diagnostics does not detect a video console, the Alpha Diagnostics uses the Debug Port interface.

### 2.1.4 Alpha SRM Console

The Alpha SRM Console firmware provides service functions commonly provided in most computers systems, including the following:

- Power-up diagnostics and initialization
- Operator interface

- OS bootstrap and restart

Alpha SRM Console firmware provides SRM support for Linux and for booting the firmware update image.

Users (operators) communicate with the SRM Console through a system console device. SRM Console firmware supports the use of either of the following:

- VT-style terminal attached to the standard serial port
- Standard VGA monitor and keyboard

SRM Console firmware provides a command line interface (CLI), or command shell. It supports both a scripting facility and one of two shells. The shell is either a simple shell for single-command line execution, or a UNIX-style shell (a subset of a Bourne shell) providing a rich set of commands and operators.

---

## 2.2 Firmware Loading Order

UP2000+ firmware loads in the following order:

1. Load SROM code firmware.
  - If system firmware is corrupted, load Alpha Diagnostics. See the *UP2000+ User Manual*, P/N 51-0042, for information on Alpha Diagnostics.
  - When SROM code firmware is loaded, go to step 2.
2. Check for configuration to enable Alpha Diagnostics.
  - If enabled, load Alpha Diagnostics. See the *UP2000+ User Manual*, P/N 51-0042, for information on Alpha Diagnostics.
  - If Alpha Diagnostics is not enabled, go to step 3.
3. Load Alpha SRM console.

SRM loads and runs the Linux kernel and its PALcode.

---

# Chapter 3 System Memory and Address Mapping

The following sections describe the UP2000+ system memory, and includes a list of valid memory configurations. Mapping information for system addresses is also provided.

---

## 3.1 Memory Subsystem

The UP2000+ has eight DIMM sockets arranged in two banks: bank 0 and bank 1. Each bank has four sockets and provides a 256-bit wide data path.

The minimum memory size is 256 MB (four 64 MB DIMMs), and the maximum size is 2 GB (eight 256 MB DIMMs). When the system clock is 83.3 MHz, the maximum bandwidth becomes 2.67 GB/sec. System firmware automatically detects memory type and size.

The UP2000+ supports the following:

- 168-pin, 100 MHz SDRAM, PLL or registered SPD DIMMs
- LVTTTL-compatible inputs and outputs
- 3.3V +/- 0.3V power supply

Each 168-pin DIMM should have eight Data Input/Output Mast (DQM) signals for each DIMM. Because there is no guarantee of all 32 loadings with DQM from the Cchip, Alpha Processor, Inc. uses a 200 psec Quick switch, part number PI3B3244, as shown in Figure 3-1.

**Note:** *DIMMs installed in one memory bank must be of the same type, size and speed. DIMMs installed in different memory banks may differ between banks, but not within a bank.*

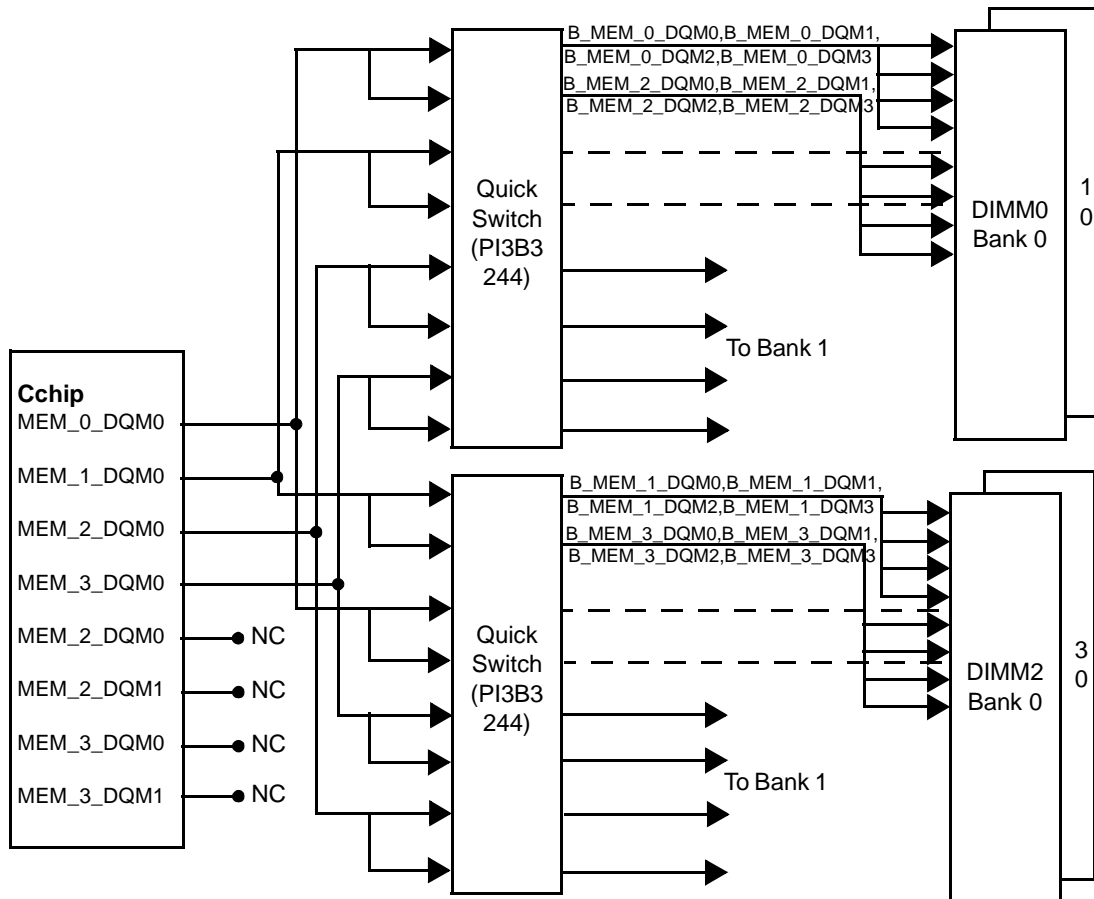


Figure 3-1 Memory DQM Configuration

## 3.2 Configuring SDRAM Memory

The UP2000+ supports memory sizes from 256 MB to 2 GB. Table 3-1 lists some of the SDRAM memory configurations available. Any combination of DIMMs that meet the 21272 configuration rules are supported by the 21272 chipset.

For a list of vendors who supply components and accessories for the UP2000+, see Appendix B.

**Table 3-1 UP2000+ SDRAM Memory Configurations**

<b>Total Memory</b>	<b>Bank 0</b>	<b>Bank 1</b>
<b>256 MB</b>	<b>64 MB x 4</b>	
512 MB	128 MB x 4	
	<b>64 MB x 4</b>	<b>64 MB x 4</b>
768 MB	128 MB x 4	64 MB x 4
<b>1 GB</b>	<b>256 MB x 4</b>	
	128 MB x 4	128 MB x 4
<b>1.5 GB</b>	<b>256 MB x 4</b>	<b>128 MB x 4</b>
2 GB	256 MB x 4	256 MB x 4

## 3.3 System Address Mapping

This section describes the mapping of the processor physical address space into memory and I/O space addresses. It also includes the translations of the processor-initiated address into a PCI address, and PCI-initiated addresses into physical memory addresses.

### 3.3.1 CPU Address Mapping to PCI Space

The physical system data bus address space is composed of the following:

- Memory address space
- Local I/O space for registers in the Cchip, Dchips, and Pchips)
- PCI space

The PCI defines four physical address spaces, as follows:

- PCI memory space (for memory residing on the PCI)
- PCI I/O space
- PCI configuration space
- PCI interrupt acknowledge cycles/PCI special cycles

Refer to Compaq's functional specification for the 21272 core logic chipset for details on the PCI space mapping.

### 3.3.2 TIGbus Address Mapping

Table 3-2 provide the address map for the TIGbus. J29, the configuration jumper, provides inputs to the TIGbus and Gpen registers.

**Table 3-2 TIGbus Address Mapping**

Capbus [23:21]	Physical Address 1	Access	Function	Comment
000	801 00xx xxx0	RW	Flash ROM address space	
001	801 08xx xxx0	RO	Gpen_0 Array0_PD[7:0]	Reserved
010	801 10xx xxx0	RO	Gpen_1 Array1_PD[7:0]	Reserved
011	801 18xx xxx0	RO	Gpen_2 Array2_PD[7:0]	Reserved
100	801 20xx xxx0	RO	Gpen_3 Array3_PD[7:0]	Reserved
101	801 28xx xxx0	RO	Gpen_4 Con_bit[7:0]	General configuration register. See Figure 3-2.
110	801 30xx x000	RO	Gpen_5 CPU0_config[7:0]	<b>CPU0 configuration register. See Figure 3-2.</b>
	801 30xx x040	RW	Flash write enable[0]	Writing a 1 to this location enables flash writes
	801 30xx xA00	RW		Reserved
	801 30xx xA40	RW		Reserved
	801 30xx x3C0	RW	CPU[1:0] HaltA	<b>Writing a 1 to either bit will halt the specified CPU.</b>
	801 30xx x5C0	RW	CPU[1:0] HaltB	Writing a 1 to either bit halts the specified CPU.
111	801 38xx x000	RO	Gpen_6 CPU1_config[7:0]	<b>CPU1 configuration register. See Figure 3-2.</b>
	801 38xx x040	RAZ	PCI_0_ok[0]	Reserved
	801 38xx x080	WO	PCI_1_ok[0]	<b>PCI0 self-test register</b>
	801 38xx x0C0	WO		PCI1 self-test register
111	801 38xx x100	RW	Soft_reset[0]	<b>To set a hardware reset for a short period of time, first write a 0, then write a 1 to this location.</b>
	801 38xx x140	RO	Tig_rev[7:0]	Bits [7:5] specify the major revision (corresponding to the board revision), [4:0] specify the minor revision.
	801 38xx x180	RO	Arbiter_rev[7:0]	<b>Bits [7:5] specify the major</b>
	801 38xx x1C0	RW	Feature_mask[7:0]	Reserved

The Gpen4 register, shown in Figure 3-2, reflects the settings of the UP2000+ Motherboard's configuration jumper, J29.

7	6	5	4	3	2	1	0
Firmware_ Config_ SW8	Reserved	BCACHE_ OFF	Fl_Wri_ Prot	Firmware_ Config_ SW4	Firmware_ Config_ SW3	Firmware_ Config_ SW2	Firmware_ Config_ SW1

**Figure 3-2 Gpen4 Register**

The Gpen5 register, shown in Figure 3-3, reflects the settings of the primary Alpha Slot B Module.

7	6	5	4	3	2	1	0
CPU0_Present_L	BC0_Config[3:0]			CPU0_Speed[2:0]			

**Figure 3-3 Gpen5 Register**

The Gpen6 register, shown in Figure 3-4, reflects the settings of the secondary Alpha Slot B Module.

7	6	5	4	3	2	1	0
CPU1_Present_L	BC1_Config[3:0]			CPU1_Speed[2:0]			

**Figure 3-4 Gpen6 Register**

# Appendix A

Alpha Slot B

Connector

Pinouts

Table A-1 describes the pinouts of the Alpha Slot B Connectors J22 and J23, which are standard Molex 74191-0002 parts.

**Table A-1 Alpha Slot B Connector Pinouts (J22, J23)**

<b>Pin</b>	<b>Signal (5V, Secondary)</b>	<b>Signal (12V, Primary)</b>	<b>Signal (5V, Secondary)</b>	<b>Signal (12V, Primary)</b>	<b>Pin</b>
A1	VTERM	VTERM	VTERM	VTERM	B1
A2	CONNECT	CONNECT	RESET_L	RESET_L	B2
A3	GND	GND	GND	GND	B3
A4	SysDataInClk_L_0	SysDataInClk_L_0	SysDataOutClk_L_0	SysDataOutClk_L_0	B4
A5	VTERM	VTERM	VTERM	VTERM	B5
A6	SysData_L_0	SysData_L_0	SysCheck_L_0	SysCheck_L_0	B6
A7	GND	GND	GND	GND	B7
A8	SysData_L_2	SysData_L_2	SysData_L_1	SysData_L_1	B8
A9	VTERM	VTERM	VTERM	VTERM	B9
A10	SysData_L_4	SysData_L_4	SysData_L_3	SysData_L_3	B10
A11	GND	GND	GND	GND	B11
A12	SysData_L_6	SysData_L_6	SysData_L_5	SysData_L_5	B12
A13	VTERM	VTERM	VTERM	VTERM	B13
A14	SysCheck_L_1	SysCheck_L_1	SysData_L_7	SysData_L_7	B14
A15	GND	GND	GND	GND	B15
A16	SysDataInClk_L_1	SysDataInClk_L_1	SysDataOutClk_L_1	SysDataOutClk_L_1	B16
A17	VTERM	VTERM	VTERM	VTERM	B17
A18	SysData_L_9	SysData_L_9	SysData_L_8	SysData_L_8	B18
A19	GND	GND	GND	GND	B19
A20	SysData_L_11	SysData_L_11	SysData_L_10	SysData_L_10	B20
A21	VTERM	VTERM	VTERM	VTERM	B21
A22	SysData_L_13	SysData_L_13	SysData_L_12	SysData_L_12	B22
A23	GND	GND	GND	GND	B23
A24	SysData_L_15	SysData_L_15	SysData_L_14	SysData_L_14	B24
A25	VTERM	VTERM	VTERM	VTERM	B25
A26	SysDataInClk_L_2	SysDataInClk_L_2	SysDataOutClk_L_2	SysDataOutClk_L_2	B26
A27	GND	GND	GND	GND	B27
A28	SysData_L_16	SysData_L_16	SysCheck_L_2	SysCheck_L_2	B28
A29	VTERM	VTERM	VTERM	VTERM	B29
A30	SysData_L_18	SysData_L_18	SysData_L_17	SysData_L_17	B30

**Table A-1 Alpha Slot B Connector Pinouts (J22, J23) (Continued)**

<b>Pin</b>	<b>Signal (5V, Secondary)</b>	<b>Signal (12V, Primary)</b>	<b>Signal (5V, Secondary)</b>	<b>Signal (12V, Primary)</b>	<b>Pin</b>
<b>A31</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>B31</b>
A32	SysData_L_20	SysData_L_20	SysData_L_19	SysData_L_19	B32
<b>A33</b>	<b>VTERM</b>	<b>VTERM</b>	<b>VTERM</b>	<b>VTERM</b>	<b>B33</b>
A34	SysData_L_22	SysData_L_22	SysData_L_21	SysData_L_21	B34
<b>A35</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>B35</b>
A36	SysCheck_L_3	SysCheck_L_3	SysData_L_23	SysData_L_23	B36
<b>A37</b>	<b>VTERM</b>	<b>VTERM</b>	<b>VTERM</b>	<b>VTERM</b>	<b>B37</b>
A38	SysDataInClk_L_3	SysDataInClk_L_3	SysDataOutClk_L_3	SysDataOutClk_L_3	B38
<b>A39</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>B39</b>
A40	SysData_L_25	SysData_L_25	SysData_L_24	SysData_L_24	B40
<b>A41</b>	<b>VTERM</b>	<b>VTERM</b>	<b>VTERM</b>	<b>VTERM</b>	<b>B41</b>
A42	SysData_L_27	SysData_L_27	SysData_L_26	SysData_L_26	B42
<b>A43</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>B43</b>
A44	SysData_L_29	SysData_L_29	SysData_L_28	SysData_L_28	B44
<b>A45</b>	<b>VTERM</b>	<b>VTERM</b>	<b>VTERM</b>	<b>VTERM</b>	<b>B45</b>
A46	SysData_L_31	SysData_L_31	SysData_L_30	SysData_L_30	B46
<b>A47</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>B47</b>
A48	ClkIn_H	ClkIn_H	ClkIn_L	ClkIn_L	B48
<b>A49</b>	<b>VTERM</b>	<b>VTERM</b>	<b>VTERM</b>	<b>VTERM</b>	<b>B49</b>
A50	FrameClk_H	FrameClk_H	FrameClk_L	FrameClk_L	B50
<b>A51</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>B51</b>
A52	SysDataInValid_L	SysDataInValid_L	SysDataOutValid_L	SysDataOutValid_L	B52
<b>A53</b>	<b>VTERM</b>	<b>VTERM</b>	<b>VTERM</b>	<b>VTERM</b>	<b>B53</b>
A54	SysFillValid_L	SysFillValid_L	ClkFwdRst_H	ClkFwdRst_H	B54
<b>A55</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>B55</b>
A56	PWROK	PWROK	PROCRDY_Srom_OE_L	PROCRDY/Srom_OE_L	B56
<b>A57</b>	<b>VTERM</b>	<b>VTERM</b>	<b>VTERM</b>	<b>VTERM</b>	<b>B57</b>
A58	SysAddIn_L_14	SysAddIn_L_14	SysAddIn_L_13	SysAddIn_L_13	B58
<b>A59</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>B59</b>
A60	SysAddIn_L_12	SysAddIn_L_12	SysAddIn_L_11	SysAddIn_L_11	B60
<b>A61</b>	<b>VTERM</b>	<b>VTERM</b>	<b>VTERM</b>	<b>VTERM</b>	<b>B61</b>
A62	SysAddIn_L_10	SysAddIn_L_10	SysAddIn_L_9	SysAddIn_L_9	B62
<b>A63</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>B63</b>

**Table A-1 Alpha Slot B Connector Pinouts (J22, J23) (Continued)**

<b>Pin</b>	<b>Signal (5V, Secondary)</b>	<b>Signal (12V, Primary)</b>	<b>Signal (5V, Secondary)</b>	<b>Signal (12V, Primary)</b>	<b>Pin</b>
A64	SysAddIn_L_8	SysAddIn_L_8	SysAddIn_L_7	SysAddIn_L_7	B64
<b>A65</b>	<b>VTERM</b>	<b>VTERM</b>	<b>VTERM</b>	<b>VTERM</b>	<b>B65</b>
A66	SysAddInClk_L	SysAddInClk_L	SysAddIn_L_6	SysAddIn_L_6	B66
<b>A67</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>B67</b>
A68	SysAddIn_L_5	SysAddIn_L_5	SysAddIn_L_4	SysAddIn_L_4	B68
<b>A69</b>	<b>VTERM</b>	<b>VTERM</b>	<b>VTERM</b>	<b>VTERM</b>	<b>B69</b>
A70	SysAddIn_L_3	SysAddIn_L_3	SysAddIn_L_2	SysAddIn_L_2	B70
<b>A71</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>B71</b>
A72	SysAddIn_L_1	SysAddIn_L_1	SysAddIn_L_0	SysAddIn_L_0	B72
<b>A73</b>	<b>VTERM</b>	<b>VTERM</b>	<b>VTERM</b>	<b>VTERM</b>	<b>B73</b>
A74	SysAddOut_L_14	SysAddOut_L_14	SysAddOut_L_13	SysAddOut_L_13	B74
<b>A75</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>B75</b>
A76	SysAddOut_L_12	SysAddOut_L_12	SysAddOut_L_11	SysAddOut_L_11	B76
<b>A77</b>	<b>VTERM</b>	<b>VTERM</b>	<b>VTERM</b>	<b>VTERM</b>	<b>B77</b>
A78	SysAddOut_L_10	SysAddOut_L_10	SysAddOut_L_9	SysAddOut_L_9	B78
<b>A79</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>B79</b>
A80	SysAddOut_L_8	SysAddOut_L_8	SysAddOut_L_7	SysAddOut_L_7	B80
<b>A81</b>	<b>VTERM</b>	<b>VTERM</b>	<b>VTERM</b>	<b>VTERM</b>	<b>B81</b>
A82	SysAddOutClk_L	SysAddOutClk_L	SysAddOut_L_6	SysAddOut_L_6	B82
<b>A83</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>B83</b>
A84	SysAddOut_L_5	SysAddOut_L_5	SysAddOut_L_4	SysAddOut_L_4	B84
<b>A85</b>	<b>VTERM</b>	<b>VTERM</b>	<b>VTERM</b>	<b>VTERM</b>	<b>B85</b>
A86	SysAddOut_L_3	SysAddOut_L_3	SysAddOut_L_2	SysAddOut_L_2	B86
<b>A87</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>B87</b>
A88	SysAddOut_L_1	SysAddOut_L_1	SysAddOut_L_0	SysAddOut_L_0	B88
<b>A89</b>	<b>VTERM</b>	<b>VTERM</b>	<b>VTERM</b>	<b>VTERM</b>	<b>B89</b>
A90	SysData_L_63	SysData_L_63	SysData_L_62	SysData_L_62	B90
<b>A91</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>B91</b>
A92	SysData_L_61	SysData_L_61	SysData_L_60	SysData_L_60	B92
<b>A93</b>	<b>VTERM</b>	<b>VTERM</b>	<b>VTERM</b>	<b>VTERM</b>	<b>B93</b>
A94	SysData_L_59	SysData_L_59	SysData_L_58	SysData_L_58	B94
<b>A95</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>B95</b>
A96	SysData_L_57	SysData_L_57	SysData_L_56	SysData_L_56	B96

**Table A-1 Alpha Slot B Connector Pinouts (J22, J23) (Continued)**

<b>Pin</b>	<b>Signal (5V, Secondary)</b>	<b>Signal (12V, Primary)</b>	<b>Signal (5V, Secondary)</b>	<b>Signal (12V, Primary)</b>	<b>Pin</b>
<b>A97</b>	<b>VTERM</b>	<b>VTERM</b>	<b>VTERM</b>	<b>VTERM</b>	<b>B97</b>
A98	SysDataInClk_L_7	SysDataInClk_L_7	SysDataOutClk_L_7	SysDataOutClk_L_7	B98
<b>A99</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>B99</b>
A100	SysCheck_L_7	SysCheck_L_7	SysData_L_55	SysData_L_55	B100
<b>A101</b>	<b>VTERM</b>	<b>VTERM</b>	<b>VTERM</b>	<b>VTERM</b>	<b>B101</b>
A102	SysData_L_54	SysData_L_54	SysData_L_53	SysData_L_53	B102
<b>A103</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>B103</b>
A104	SysData_L_52	SysData_L_52	SysData_L_51	SysData_L_51	B104
<b>A105</b>	<b>VTERM</b>	<b>VTERM</b>	<b>VTERM</b>	<b>VTERM</b>	<b>B105</b>
A106	SysData_L_50	SysData_L_50	SysData_L_49	SysData_L_49	B106
<b>A107</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>B107</b>
A108	SysData_L_48	SysData_L_48	SysCheck_L_6	SysCheck_L_6	B108
<b>A109</b>	<b>VTERM</b>	<b>VTERM</b>	<b>VTERM</b>	<b>VTERM</b>	<b>B109</b>
A110	SysDataInClk_L_6	SysDataInClk_L_6	SysDataOutClk_L_6	SysDataOutClk_L_6	B110
<b>A111</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>B111</b>
A112	SysData_L_47	SysData_L_47	SysData_L_46	SysData_L_46	B112
<b>A113</b>	<b>VTERM</b>	<b>VTERM</b>	<b>VTERM</b>	<b>VTERM</b>	<b>B113</b>
A114	SysData_L_45	SysData_L_45	SysData_L_44	SysData_L_44	B114
<b>A115</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>B115</b>
A116	SysData_L_43	SysData_L_43	SysData_L_42	SysData_L_42	B116
<b>A117</b>	<b>VCC_CORE</b>	<b>VCC_CORE</b>	<b>VCC_CORE</b>	<b>VCC_CORE</b>	<b>B117</b>
A118	SramPowerLevel	SramPowerLevel	Core_PowerGood	Core_PowerGood	B118
<b>A119</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>B119</b>
A120	SysData_L_41	SysData_L_41	SysData_L_40	SysData_L_40	B120
<b>A121</b>	<b>VCC</b>	<b>VCC</b>	<b>VCC</b>	<b>VCC</b>	<b>B121</b>
A122	SysDataInClk_L_5	SysDataInClk_L_5	SysDataOutClk_L_5	SysDataOutClk_L_5	B122
<b>A123</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>B123</b>
A124	SysCheck_L_5	SysCheck_L_5	SysData_L_39	SysData_L_39	B124
<b>A125</b>	<b>VCC_SRAM</b>	<b>VCC_SRAM</b>	<b>VCC_SRAM</b>	<b>VCC_SRAM</b>	<b>B125</b>
A126	SysData_L_38	SysData_L_38	SysData_L_37	SysData_L_37	B126
<b>A127</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>B127</b>
A128	SysData_L_36	SysData_L_36	SysData_L_35	SysData_L_35	B128
<b>A129</b>	<b>V33</b>	<b>V33</b>	<b>V33</b>	<b>V33</b>	<b>B129</b>

**Table A-1 Alpha Slot B Connector Pinouts (J22, J23) (Continued)**

<b>Pin</b>	<b>Signal (5V, Secondary)</b>	<b>Signal (12V, Primary)</b>	<b>Signal (5V, Secondary)</b>	<b>Signal (12V, Primary)</b>	<b>Pin</b>
A130	SysData_L_34	SysData_L_34	SysData_L_33	SysData_L_33	B130
<b>A131</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>B131</b>
A132	SysData_L_32	SysData_L_32	SysCheck_L_4	SysCheck_L_4	B132
<b>A133</b>	<b>V33</b>	<b>V33</b>	<b>V33</b>	<b>V33</b>	<b>B133</b>
A134	SysDataInClk_L_4	SysDataInClk_L_4	SysDataOutClk_L_4	SysDataOutClk_L_4	B134
<b>A135</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>B135</b>
A136	SromClk_H	SromClk_H	SromData_H	SromData_H	B136
<b>A137</b>	<b>V33</b>	<b>V33</b>	<b>V33</b>	<b>V33</b>	<b>B137</b>
A138	SRAM_ZZ	SRAM_ZZ	CORE_PWREN	CORE_PWREN	B138
<b>A139</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>B139</b>
A140	FIDSEL_L_0	FIDSEL_L_0	FIDSEL_L_1	FIDSEL_L_1	B140
<b>A141</b>	<b>V33</b>	<b>V33</b>	<b>V33</b>	<b>V33</b>	<b>B141</b>
A142	APIC_CLK	APIC_CLK	APIC_DATA_0	APIC_DATA_0	B142
<b>A143</b>	<b>VP12</b>	<b>VP12</b>	<b>VP12</b>	<b>VP12</b>	<b>B143</b>
A144	APIC_DATA_1	APIC_DATA_1	FERR	FERR	B144
<b>A145</b>	<b>VRM_SOURCE_POWER (5V)</b>	<b>VRM_SOURCE_POWER (12V)</b>	<b>VRM_SOURCE_POWER (5V)</b>	<b>VRM_SOURCE_POWER (12V)</b>	<b>B145</b>
A146	ALPHA_H/K7_L	ALPHA_H/K7_L	CPU_Present	CPU_Present	B146
<b>A147</b>	<b>VRM_SOURCE_POWER (5V)</b>	<b>VRM_SOURCE_POWER (12V)</b>	<b>VRM_SOURCE_POWER (5V)</b>	<b>VRM_SOURCE_POWER (12V)</b>	<b>B147</b>
A148	FID_0	FID_0	FID_1	FID_1	B148
<b>A149</b>	<b>VRM_SOURCE_POWER (5V)</b>	<b>VRM_SOURCE_POWER (12V)</b>	<b>VRM_SOURCE_POWER (5V)</b>	<b>VRM_SOURCE_POWER (12V)</b>	<b>B149</b>
A150	FID_2	FID_2	FID_3	FID_3	B150
<b>A151</b>	<b>VRM_SOURCE_POWER (5V)</b>	<b>VRM_SOURCE_POWER (12V)</b>	<b>VRM_SOURCE_POWER (5V)</b>	<b>VRM_SOURCE_POWER (12V)</b>	<b>B151</b>
A152	I2C_ADDR_0	I2C_ADDR_0	I2C_ADDR_1	I2C_ADDR_1	B152
<b>A153</b>	<b>VRM_SOURCE_POWER (5V)</b>	<b>VRM_SOURCE_POWER (12V)</b>	<b>VRM_SOURCE_POWER (5V)</b>	<b>VRM_SOURCE_POWER (12V)</b>	<b>B153</b>
A154	I2C_ADDR_2	I2C_ADDR_2	I2C_INTR_L	I2C_INTR_L	B154
<b>A155</b>	<b>VRM_SOURCE_POWER (5V)</b>	<b>VRM_SOURCE_POWER (12V)</b>	<b>VRM_SOURCE_POWER (5V)</b>	<b>VRM_SOURCE_POWER (12V)</b>	<b>B155</b>
A156	I2C_SCLK	I2C_SCLK	I2C_SDA	I2C_SDA	B156
<b>A157</b>	<b>VRM_SOURCE_POWER (5V)</b>	<b>VRM_SOURCE_POWER (12V)</b>	<b>VRM_SOURCE_POWER (5V)</b>	<b>VRM_SOURCE_POWER (12V)</b>	<b>B157</b>
A158	INIT_L	INIT_L	IGNNE_L	IGNNE_L	B158
<b>A159</b>	<b>VRM_SOURCE_POWER (5V)</b>	<b>VRM_SOURCE_POWER (12V)</b>	<b>VRM_SOURCE_POWER (5V)</b>	<b>VRM_SOURCE_POWER (12V)</b>	<b>B159</b>

**Table A-1 Alpha Slot B Connector Pinouts (J22, J23) (Continued)**

<b>Pin</b>	<b>Signal (5V, Secondary)</b>	<b>Signal (12V, Primary)</b>	<b>Signal (5V, Secondary)</b>	<b>Signal (12V, Primary)</b>	<b>Pin</b>
A160	IRQ_H_0/NMI	IRQ_H_0/NMI	IRQ_H_1/INTR	IRQ_H_1/INTR	B160
<b>A161</b>	<b>VRM_SOURCE_POWER (5V)</b>	<b>VRM_SOURCE_POWER (12V)</b>	<b>VRM_SOURCE_POWER (5V)</b>	<b>VRM_SOURCE_POWER (12V)</b>	<b>B161</b>
A162	IRQ_H_2/SMI_L	IRQ_H_2/SMI_L	IRQ_H_3/STPCLK_L	IRQ_H_3/STPCLK_L	B162
<b>A163</b>	<b>VRM_SOURCE_POWER (5V)</b>	<b>VRM_SOURCE_POWER (12V)</b>	<b>VRM_SOURCE_POWER (5V)</b>	<b>VRM_SOURCE_POWER (12V)</b>	<b>B163</b>
A164	IRQ_H_4/SCIINT_L	IRQ_H_4/SCIINT_L	IRQ_H_5/A20M_L	IRQ_H_5/A20M_L	B164
<b>A165</b>	<b>VRM_SOURCE_POWER (5V)</b>	<b>VRM_SOURCE_POWER (12V)</b>	<b>VRM_SOURCE_POWER (5V)</b>	<b>VRM_SOURCE_POWER (12V)</b>	<b>B165</b>

# Appendix B

Support,

Products and

Documentation

## B.1 Customer Support

Alpha Processor, Inc. provides assistance for their products on their web page at [www.alpha-processor.com](http://www.alpha-processor.com).

Alpha Original Equipment Manufacturers (OEMs) provide the following web page resources for customer support:

URL	Description
<a href="http://www.compaq.com">http://www.compaq.com</a>	Contains links for the 21272 chipset.
<a href="http://www.samsungsemi.com">http://www.samsungsemi.com</a>	Contains links for the 21264 CPU.

## B.2 Supporting Products

Alpha Processor, Inc. maintains a Hardware Compatibility List on their website for components and accessories that are not included with the UP2000+. Compatibility for items such as memory, power supplies, and enclosure are listed.

Point your browser to [www.alpha-processor.com](http://www.alpha-processor.com) and check the Product Information list for Peripherals.

## B.3 Alpha Products

Alpha Processor, Inc. maintains information about other Alpha products on their website. Point your browser to [www.alpha-processor.com](http://www.alpha-processor.com) and check the Product Information list for Alpha products.

## B.4 Documentation

### B.4.1 Alpha Documentation

Title	Vendor
<b><i>Alpha Architecture Reference Manual, Third Edition</i></b>	<b>Compaq Computer Corporation, Digital Press order# EQ-W938E-DP</b>
<i>Alpha Architecture Handbook, Version 4</i>	Compaq Computer Corporation Digital Press order# EC-QD2KC-TE
<b><i>AlphaPC 264DP Technical Reference Manual</i></b>	<b>Compaq Computer Corporation, Digital Press order# EC-RBODA-TE</b>
<i>UP2000+ Quick Start Installation Guide (51-0041)</i>	Alpha Processor, Inc.
<b><i>UP2000+ User Manual (51-0042)</i></b>	<b>Alpha Processor, Inc.</b>
<i>MACASE Chassis RFI Upgrade Kit Application Note (51-0038)</i>	Alpha Processor, Inc.

### B.4.2 Third Party Documentation

You can order the following associated documentation directly from the vendor.

Title	Vendor
<ul style="list-style-type: none"> <li>• <b><i>PCI Local Bus Specification, Revision 2.1</i></b></li> <li>• <b><i>PCI Multimedia Design Guide, Revision 1.0</i></b></li> <li>• <b><i>PCI System Design Guide</i></b></li> <li>• <b><i>PCI-to-PCI Bridge Architecture Specification, Revision 0</i></b></li> <li>• <b><i>PCI BIOS Specification, Revision 2.1</i></b></li> </ul>	<b>PCI Special Interest Group</b> U.S. 1-800-433-5177 International 1-503-797-4207 FAX 1-503-234-6762
<i>Computer Architecture</i>	John L. Hennessy and David A. Patterson, Morgan Kaufman Publishers, San Mateo, CA, 1990

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